IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UTILITY PATENT APPLICATION TRANSMITTAL LETTER

Attorney Docket No.: ONS00114

To: Assistant Commissioner for Patents
Box Patent Application
Washington D.C., 20231

Dear Sir:

Transmitted herewith for filing under 37 C.F.R. 1.53(b) is a Nonprovisional Utility Patent Application:

☒ New Application; or

☐ Continuation; or ☐ Divisional; or ☐ Continuation-In-Part (CIP); of prior US Application No. ________________, filed on ___________, having U.S. Examiner ____________, in Group Art Unit _________

Of: Misbahul Azam, Jeffrey Pearse, and Christopher J. Gass

For: **TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY**

☒ 3 sheets of INFORMAL drawings and 15 pages of specification and claims.

☒ Newly executed oath or declaration combined with Power of Attorney on 4 pages.

☐ Copy of oath or declaration from prior U.S. application serial no. ______________________
☐ The following named inventor(s) from the prior application are hereby deleted from this application in accordance with 37 C.F.R. 1.63(d)(2) and 1.33(b): ____.

☐ A certified copy of a ___________ (non-US) application serial number __________, having a filing date of __________, and foreign priority to this non-US application for the present application is hereby claimed under 35 USC 119.

☒ An Assignment Transmittal Letter and Assignment of the invention to Semiconductor Components Industries, LLC

☐ An Information Disclosure Statement (IDS), with PTO-1449, and _______ citation copies.

☒ Return Receipt Postcard.

☐ Preliminary Amendment.

☐ Please cancel pending claims __________.

☐ Incorporation by Reference (for Continuation/Division/CIP application). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by

reference therein. Since the present application is based on a prior US application, please amend the specification by adding the following sentence before the first sentence of the specification:

"The present application is based on prior US application No. _______, filed on______ _____, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed."

☐ Applicant hereby petitions pursuant to 37 C.F.R. §1.136(a) for a ________ month extension of time for response to the outstanding Official Action mailed ____________. The period for response was previously set to elapse __________, and is accordingly hereby extended to _ __, which is still within the six-month statutory period for response (35 U.S.C. § 133) which elapses ________. The reason for this petition is that a Division, Continuation, or CIP is being filed, and it is desired to maintain the present application in pending condition pursuant to 35 USC § 120 through at least the filing of the Division, Continuation, or CIP application. The required Extension Fee established by 37 C.F.R. § 1.17(a) pursuant to 35 U.S.C. § 41(a) (8) is:

EXTENSION	FEE
☐ First Month	$110.00
☐ Second Month	$380.00
☐ Third Month	$870.00
☐ Fourth Month	$1,360.00
☐ Fifth Month	$1,850.00

☒ The filing fee is calculated as follows:

CLAIMS AS FILED, LESS ANY CANCELED BY AMENDMENT

FOR	NUMBER OF CLAIMS	NUMBER EXTRA	RATE		FEE
TOTAL CLAIMS	27 - 20 =	7	x $18	=	$ 126.00
INDEPENDENT CLAIMS	4 - 3 =	1	x $80	=	$ 80.00
MULTIPLE DEPENDENT CLAIMS			$260	=	$ 0.00
BASIC FEE				=	$ 710.00
TOTAL FILING FEE				=	$ 916.00

☒ Please charge Deposit Account No. 501086 in the amount of $ 916.00 for the Total Filing Fee, and the Extension Fee under 37 C.F.R. §1.136(a), if applicable.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required now or in the future during the entire pendency of this application under 37 C.F.R. 1.16 or 37 C.F.R. 1.17, including any present or future time extension fees which may be required, or credit any overpayment to Deposit Account No. 501086.

☒ This sheet is submitted in triplicate.

This transmittal letter has 3 total pages.

Application Transmittal 1.53(b)

PATENT
ONS00114

10/31/00
DATE

Robert D. Atkins 34,288
Robert D. Atkins REG. NO.

Semiconductor Components Industries, LLC
Patent Administration Dept - MD A230
P.O. Box 62890
Phoenix, AZ 85082-2890

Attorney of Record
Telephone No.: (602) 244-3419
Facsimile No.: (602) 244-5601

TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY

BACKGROUND OF THE INVENTION

The present invention relates in general to trench semiconductor devices and, more particularly, to methods of forming trenches in a semiconductor devices.

Trench semiconductor devices are used in many applications including power supplies, battery chargers, computers, and cell phones. During the process used to manufacture trench semiconductor devices a dry silicon etch step is used to form the trenches in a silicon material of the semiconductor device. However, the channel region inside the trench wall of the semiconductor device is frequently damaged and rough edges can be formed after the dry silicon etch step. The damage to the channel region can cause leakage which then causes reduced carrier lifetime in the channel area. Decreased carrier lifetime increases the voltage threshold thereby increasing the on-state resistance of the semiconductor device. There is conventional prior art cleaning processes used to reduce the damage to the trench wall of the semiconductor device, but is at the cost of extra process steps. However, the extra process steps used to remove the damage to the trench walls frequently does not completely anneal the trench walls leaving the damage to the channel region in the semiconductor device.

Furthermore, the trench depth of a semiconductor device is typically a critical dimension which is difficult to meet using the dry silicon etch process.

For example, a trench power MOSFET device should have the trench depth just below the diffused body region to minimize the gate to drain capacitance and minimize the gate oxide electric field strength.

Accordingly, it is desirable to have a manufacturing process to form trenches in a semiconductor device without causing damage to the trench. Further, it is desirable to have the manufacturing process provide an accurate alignment of the trench bottom to specific dopant distribution during the process steps. The invention disclosed herein will address the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a semiconductor device in a manufacturing step illustrating a masking step;

FIG. 2 is a cross-sectional view of the semiconductor device in the manufacturing step after an etching step;

FIG. 3 is a cross-sectional view of the semiconductor device in the manufacturing step illustrating a blanket epi growth technique;

FIG. 4 is a cross-sectional view of the semiconductor device in the manufacturing step illustrating a selective epi growth technique;

FIG. 5 is a cross-sectional view of a plurality of trenches in the semiconductor device; and

FIG. 6 is a cross-sectional view of a semiconductor device in the final stage of manufacturing using the process disclosed herein.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional view of a semiconductor device in a process step of a manufacturing process. FIG. 1 can be a metal oxide semiconductor field effect transistor (MOSFET) or an insulated gate bipolar transistor (IGBT). It will be apparent to someone skilled in the art that the process disclosed herein can be used to manufacture any one of these semiconductor devices. The method of making an n-channel MOSFET device is disclosed herein to illustrate the preferred process. However, the process can easily be used to make a p-channel MOSFET device.

A typical n-channel MOSFET semiconductor device shown in FIG. 1 includes foundation layer 12 grown on substrate 10. Foundation layer 12 is typically a lightly doped n-type silicon of typically $5x10^{16}$ atoms per cm^3 with dimensions in the range of five to fifty microns in thickness. Dimensions are determined for foundation layer 12 based on application. A thick layer ranging from twenty to thirty microns is typically used for foundation layer 12 for high voltage applications, where as a smaller thickness is used for low voltage applications. Substrate 10 is typically a highly doped n-type substrate of arsenic or phosphorous. A first layer, masking material 14, is grown on foundation layer 12. Masking material 14 is typically an oxide material, i.e. silicon dioxide, grown using a thermal oxide or can be deposited. A nitride material can also be used for masking material 14. Mask 16 is formed on masking material 14 where a trench is desired in the semiconductor device. Any typical photoresist material known to someone skilled in the art can be used for mask

16. An etch step is used to remove portions of masking material 14 where mask 16 is not formed leaving protruding portion 18 as shown in FIG. 2. Protruding portion 18 is a protruding portion of masking material 14 remaining after the etch step. Thus, protruding portion 18 will be made of a material of either silicon dioxide or nitride.

A dry etch process or any other similar process known to those skilled in the art is used in the etch step to remove portions of masking material 14. During this point in the process, an implant, implant 22, can be formed in foundation layer 12 at opening 20 shown in FIG. 2. Typically, implant 22 added at this point in the process is used for an IGBT device. An IGBT semiconductor device typically has a very low resistance, and as such turns off slowly. Adding implant 22 can modify and improve the turn-off of the IGBT semiconductor device. Implant 22 is formed in foundation layer 12. Implant 22 would typically be titanium or germanium. For an IGBT, foundation layer 12 would be a lightly doped n-type region.

A second layer, epi layer 24, is grown on foundation layer 12 adjacent to protruding portion 18 at opening 20 as shown in FIG. 3. Epi layer 24 is typically lightly doped p-type silicon of approximinatly 5×10^{17} atoms per cm^3. The growth of epi layer 24 is temperature controlled so that the layer only grows vertically above foundation layer 12 and not over protruding portion 18. For example, if foundation layer 12 is silicon and protruding portion 18 is oxide, the growth of epi layer 24 will only grow vertically where the silicon is exposed, and not where the oxide is exposed. Thus, epi layer 24 does not nucleate over the oxide material of protruding portion

18. The growth technique typically used to grow epi layer 24 is a selective epitaxial growth (SEG) process which is commonly known to someone skilled in the art. A cleaning polishing step is typically done after the SEG step to further smooth the surfaces of epi layer 24 and protruding portion 18.

An alternative to the SEG technique, is a blanket epitaxial growth (BEG) process which grows epi layer 24 as shown in FIG. 4. Epi layer 24 is grown over foundation layer 12 and protruding portion 18 using BEG. Epi layer 24 of FIG. 4 is polished back to ensure that protruding portion 18 is planarized with epi layer 24 as shown in FIG. 3. A polish step common to someone skilled in the art is chemical or mechanical polish (CMP). The BEG process grows an amorphous material such as a polysilicon material over protruding portion 18 and a crystalline material such as silicon over the exposed portions of foundation layer 12.

After the growth technique and polish step described above is completed, a non-damaging mask removal is used to remove protruding portion 18. Typically, the non-damaging mask removal technique is a wet oxide etch process. The wet oxide etch process is commonly known to someone skilled in the art as having a good selectivity between oxide and silicon material. Thus, the wet oxide etch process is used to remove protruding portion 18 to form trench 26 as shown in FIG. 5. The resulting trench 26 typically has squared corners at the junction to epi layer 24 and foundation layer 12. A silicon wet etch process is used to round off the corners at edge 28 of trench 26 shown in FIG. 5. Any other suitable wet etch process can be used to round off the corners as will be appreciated to someone skilled in the art. At this point

in the process implant 30 can be formed below trench 26 in foundation layer 12 as shown in FIG. 5. Implant 30 will typically be formed below trench 26 when making a MOSFET semiconductor device. The MOSFET semiconductor device has two parameters which can be modified using implants below the trench of the MOSFET. Namely, a lower device resistance, and an increase in the breakdown voltage. The device resistance can be reduced in a MOSFET semiconductor device by adding, for example, a phosphorous implant for implant 30. To raise the breakdown voltage of a MOSFET semiconductor device an implant of, for example, boron can be used for implant 30. The use of the above implants is typically known to someone skilled in the art, and is shown to illustrate the ease of using implants with the technique disclosed herein.

FIG. 6 illustrates a complete MOSFET semiconductor device formed using the above process. Once trench 26 is formed using the process, gate oxide layer 32 is disposed within trench 26. Gate oxide layer 32 is typically one to three hundred Angstroms in thickness. Gate structure 34 is disposed above gate oxide layer 32 within trench 26. Gate structure 34 is typically formed from a highly doped polysilicon with phosphorus of typically $2x10^{19}$ to $3x10^{19}$ atoms per cm^3. Source region 36 is typically a heavily doped n-type region formed within epi layer 24 adjacent to trench 26. Source region 36 is typically a shallow region of two tenths um in thickness. A typical dopant for source region 36 is an n-type arsenic doped region. Epi layer 24 further includes doped region 38 which is a heavily doped p-type region extending from the surface of epi layer 24. Doped region 38 typically has a higher doping

concentration than epi layer 24. Doped region 38 is typically formed to a depth of two to five tenths um and provides a low contact resistance between metal electrode layer 40 and epi layer 24. A typical dopant for doped region 38 is boron. ILD layer 42 is disposed on the top surface of epi layer 24 above gate structure 34 and source region 36. ILD layer 42 is typically silicon dioxide of approximately five thousand angtroms, and provides an isolation between metal electrode layer 40 and gate structure 34. Metal electrode layer 40 is formed above ILD layer 42 and on the top surface of epi layer 24 to provide a low resistive contact to source region 36 and doped region 38. Metal electrode layer 40 is typically an aluminum material.

It should be apparent to someone skilled in the art that the above process automatically aligns the depth of trench 26 to major surface 30 of foundation layer 12 as shown in FIG. 5. Prior art methods do not allow for an easy alignment of a trench and an epitaxial layer of a semiconductor device. The trench of a semiconductor device can be cut either too deep or too shallow. The process described herein provides a way to control the trench depth to avoid this problem. For example, in a power MOSFET device the optimum depth of a trench is at the interface between foundation layer 12 and masking material 14 as shown in FIG. 1. If the depth is too shallow the power MOSFET device will not work since no channel is formed, and if the depth is too deep, i.e. to far into foundation layer 12, the device will experience breakdown problems.

The following is an example in using the above described process. For example, it is desired to form a one micron deep trench for trench 26 using a five micron

thick foundation layer 12 to form the epitaxial layer of the semiconductor device. In the prior art, the dry etch process would be used to form the one micron deep trench in a five micron thick epitaxial layer by removing a one micron deep section of material from the five micron thick epitaxial layer. The prior art process produces two problems. First, the trench depth is difficult to control, and secondly, the resulting trench walls become damaged from the dry etch process. The process described herein mediates the above described problems in forming trench semiconductor devices. To form the same one micron deep trench, the process described herein starts with a four micron thick, for example, lightly doped n-type foundation layer 12. A one micron thick masking material 14, for example, silicon dioxide is grown on the four micron thick foundation layer 12. Mask 16 is formed on masking material 14 using photoresist at regions where a trench is desired as shown in FIG. 1. An etch step removes all of masking material 14 except at regions where mask 16 were formed. The etch step leaves a one micron thick protruding portion 18 as shown in FIG. 2. A dry etch process or any other type of process to those skilled in the art is used in the etch step. A one micron thick epi layer 24, using silicon for example, is grown on foundation layer 12 adjacent to protruding portion 18 at opening 20 as shown in FIG. 3. Epi layer 24 is grown using either the SEG or BEG process as described previously, and is typically well known to someone skilled in the art. The SEG process results in a one micron thick growth of silicon for epi layer 24. The BEG process requires a CMP to polish back epi layer 24 to planarize it with protruding portion 18 to form a one micron thick epi layer 24.

A wet oxide etch process is used to remove the one micron thick lightly doped n-type protruding portion 18, and leaving the one micron thick epi layer 24 of silicon. The wet oxide etch process is common to those skilled in the art. Thus, the etch process is not limited to the process described herein, and any other type of process can easily be used. The wet oxide etch process leaves a one micron deep trench 26 within the silicon of epi layer 24 as shown in FIG. 5. To complete the process, a silicon wet etch process is used to round off the corners shown in FIG. 5 at edge 28 of the one micron deep trench 26. The remaining process steps to complete the semiconductor device shown in FIG. 6 is known to someone skilled in the art.

Thus, the method of forming a trench in a semiconductor device described herein provides a process to form a trench without causing damage to the trench walls. The prior art processes typically cause trench wall damage by etching out the desired trench, where the process described herein builds the trench thereby eliminating trench wall damage. Further, the disclosed process provides accurate alignment of the trench bottom to specific dopant distributions formed in a semiconductor device.

CLAIMS

What is claimed is:

1. A method of forming a trench in a semiconductor device, comprising:

disposing a masking material on the semiconductor device;

forming a protruding portion at a location of the trench by forming an opening in the masking material adjacent to the location of the trench;

depositing a semiconductor material to fill in the opening; and

removing the protruding portion to form the trench.

2. The method of claim 1, further includes:

providing a substrate supporting the masking material; and

forming a first epi layer between the substrate and the masking material.

3. The method of claim 1, wherein the semiconductor material is an epitaxial material.

4. The method of claim 1, further including the step of forming a mask at the location of the trench after disposing the masking material.

5. The method of claim 4, wherein forming the protruding portion further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

6. The method of claim 1, wherein depositing the semiconductor material includes using a selective epi growth process to fill in the opening.

7. The method of claim 1, wherein depositing the semiconductor material includes using a blanket epi growth process to deposit the semiconductor material over the protruding portion and in the opening.

8. The method of claim 1, wherein removing the protruding portion step is a non-damaging mask removal step.

9. A method of forming a trench in a semiconductor device, comprising:

providing a substrate for the semiconductor device;

forming a first epi layer above the substrate and having a major surface;

forming a protruding region on the first epi layer having an opening adjacent to the protruding region and exposing the major surface of the first epi layer;

forming a second epi layer within the opening adjacent to the protruding region; and removing the protruding region to form the trench within the second epi layer aligned with the major surface of the first epi layer of the semiconductor device.

10. The method of claim 9, further including before forming the protruding region, forming a masking material above the first epi layer.

11. The method of claim 10, further including forming a mask on the masking material at a location for the trench;

12. The method of claim 11, wherein the mask is a photoresist material.

13. The method of claim 11, wherein forming the protruding region further includes performing an etch step to remove the masking material where the mask is absent to form the opening.

14. The method of claim 9, wherein forming the second epi layer includes using a selective epi growth process.

15. The method of claim 9, wherein forming the second epi layer further includes forming the second epi layer over the protruding region.

16. The method of claim 15, wherein forming the second epi layer over the protruding region includes using a blanket epi growth process.

17. A method of forming a trench in a semiconductor device, comprising;

disposing a first material on the semiconductor device;

forming first and second openings in the first material to form a protruding region; and

disposing a second material in the first and second openings; and

removing the protruding region to form the trench.

18. The method of claim 17, further including:
forming a substrate below the first material; and
forming an epi layer between the substrate and the first material.

19. The method of claim 17, wherein the first material is a masking material from a group consisting of silicon dioxide and silicon nitride.

20. The method of claim 17, wherein the second material is an epitaxial material comprised of silicon.

21. The method of claim 17, further including forming a mask on the first material after disposing the first material.

22. The method of claim 21, wherein forming the first and second openings includes performing an etch step to remove the first material adjacent to the mask.

23. The method of claim 17, wherein disposing the second material includes using a selective epi growth process.

24. The method of claim 17, wherein disposing the second material further includes disposing the second material over the protruding region.

25. The method of claim 24, wherein diposing the second material over the protruding region includes using a blanket epi growth process.

26. A semiconductor device having a semiconductor material body, comprising:

an epitaxial layer disposed above the semiconductor material body;

a trench formed within the epitaxial layer where a bottom surface of the trench is aligned with an interface between the epitaxial layer and the semiconductor material body; and

a gate structure disposed within the trench to form the semiconductor device.

27. The semiconductor device of claim 26, further including:

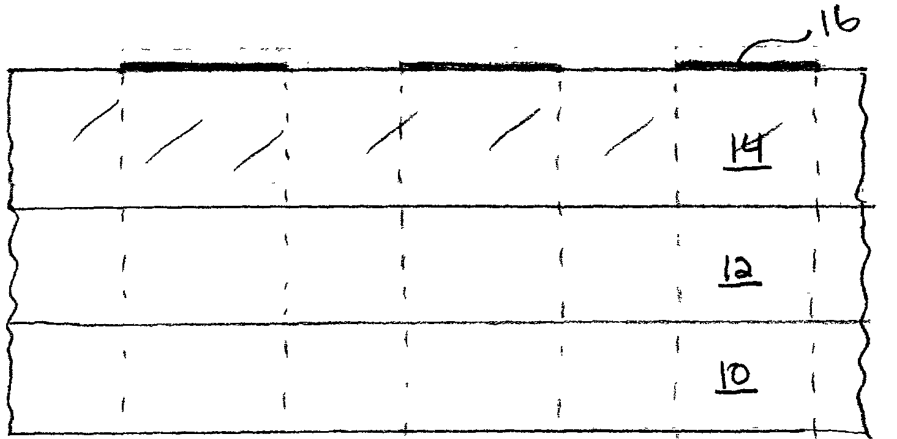
a source region formed within the expitaxial layer; and

a p-type region adjacent to the source region in the epitaxial layer.

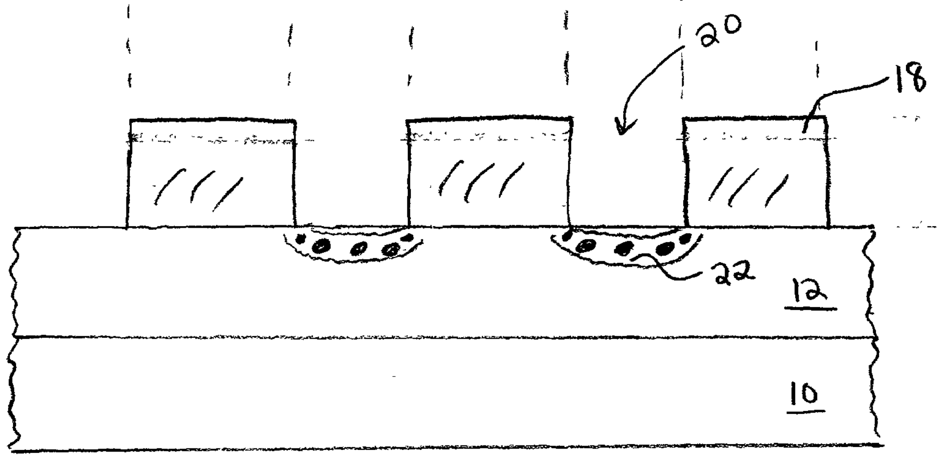
TRENCH GROWTH TECHNIQUES
USING SELECTIVE EPITAXY

Abstract of the Disclosure

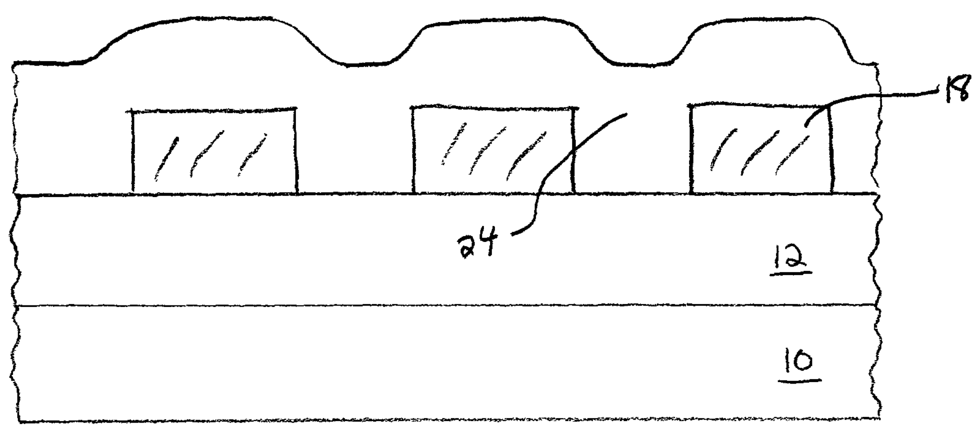
A masking material (14) is formed on a foundation layer (12) and a substrate (10). A mask (16) is disposed onto the masking material (14) where a trench (26) is desired to be formed. An etch step removes all of the masking material (14) except at regions where the mask (16) was formed leaving a protruding portion (18) with an opening (20) on either side. An epi layer (24), is grown on the foundation layer (12) adjacent to the protruding portion (18) in the opening (20). A wet oxide etch process is used to remove the protruding portion (18) leaving a trench (26) formed in the epi layer (24). To complete the process, a silicon wet etch process is used to round off the corners at an edge (28) of the trench (26).



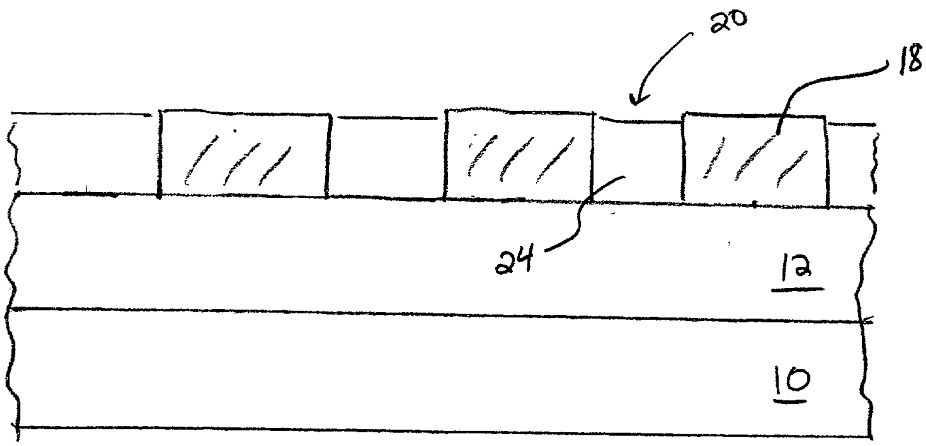
- FIG 1 -



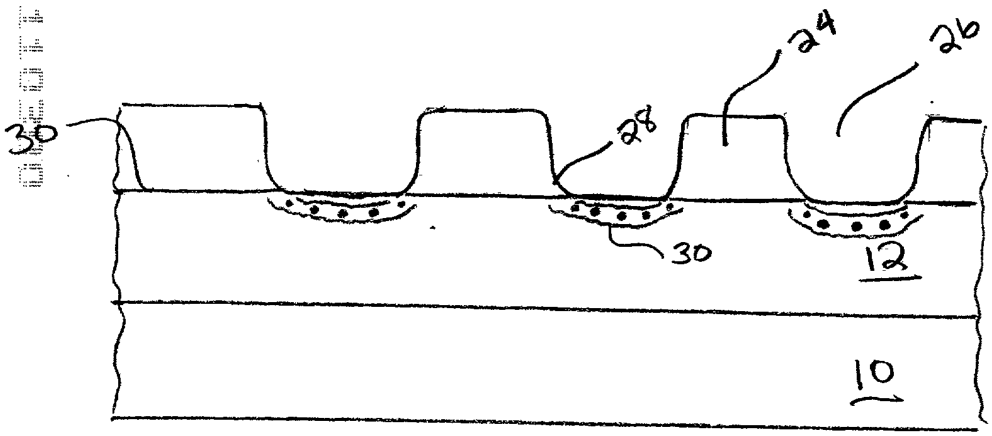
- FIG 2 -



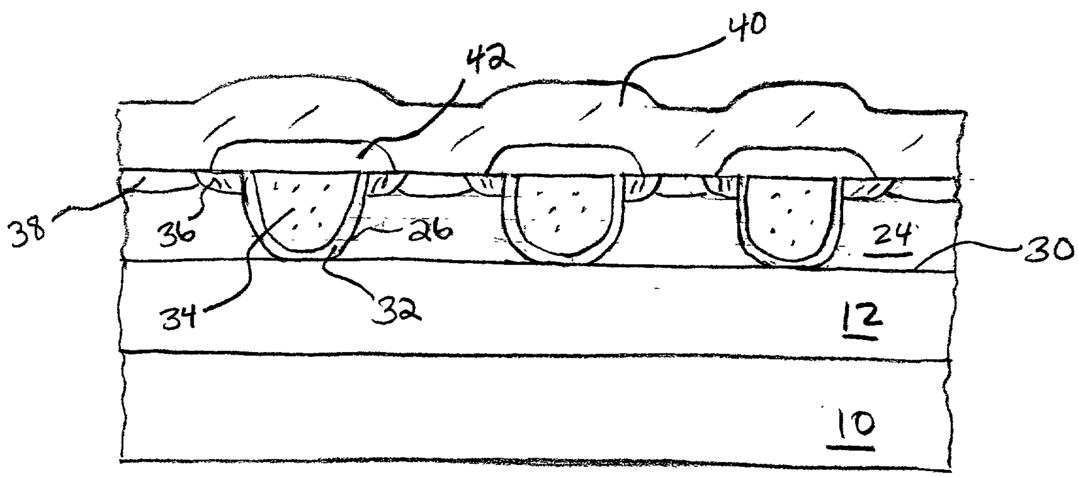
- FIG 4 -



-FIG 3-



-FIG 5-



-FIG. 6-

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket ONS00114

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY, the specification of which is attached hereto unless the following box is checked:

☐ Application was filed on ______________________
as Application No. ______________________
and was amended on ______________________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal

Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith:

Robert D. Atkins, Reg. No. 34,288; Michael T. Wallace, Reg. No. 45,420.

Address all telephone calls to Mr. Erick W. Seltmann at telephone no. (602) 244-4885.

Address all correspondence to Robert D. Atkins, Semiconductor Components Industries, LLC, Patent Administration Dept - MD A230, P.O. Box 62890, Phoenix, AZ 85082-2890.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST INVENTOR: FIRST MIDDLE LAST	INVENTOR'S SIGNATURE:	DATE:
Misbahul Azam		10/25/00
RESIDENCE: 424 West Fabens Lane, Gilbert, AZ 85233		CITIZENSHIP: United States
POST OFFICE ADDRESS: Same as above		

PATENT
ONS00114

FULL NAME OF SECOND INVENTOR: FIRST MIDDLE LAST	INVENTOR'S SIGNATURE:	DATE:
Jeffrey Pearse		25 Oct 2000

RESIDENCE:	CITIZENSHIP:
1822 West Alamo Dr, Chandler, AZ 85224	United States

POST OFFICE ADDRESS.
Same as above

FULL NAME OF THIRD INVENTOR: FIRST MIDDLE LAST	INVENTOR'S SIGNATURE.	DATE:
Christopher J. Gass		30/oct/2000
RESIDENCE: 564 West Minton Drive, Tempe, AZ 85282		CITIZENSHIP: United States
POST OFFICE ADDRESS. Same as above		